

# A Low Cost SVPWM Controller for Five-Phase VSI Using PIC18F4550

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**Abstract**— The development in the technology of power electronic switches has considerably reduced the restriction on the number of phases of a Voltage Source Inverter (VSI) design. In this paper, a design of an algorithm using sectorless space vector pulse width modulation (SVPWM) technique is worked out and based on the same, control of a five phase VSI and its implementation is focused. For higher reliability and improved performance, the third harmonic component can be utilized with the fundamental component for five phase induction motors, in standalone applications. A computationally efficient SVPWM algorithm for a five phase VSI is developed and tested using MATLAB / SIMULINK. This algorithm is implemented with a low cost circuitry using PIC18F4550 and the experimental results are also presented.

**Index Terms**— Harmonics, PIC, Pulse Width Modulation, Space Vector and VSI

## I. INTRODUCTION

High power applications demand converters which are capable to conduct large current to meet the load requirements. However, the current rating of the converters cannot be increased beyond a particular limit due to the limitation imposed by the semiconductor devices. Hence, there is a necessity for a power converter with high current carrying capability. This need can be satisfied by the use of multi phase converters [1]. Multi phase converters have come into existence due to the rapid growth of power electronics which has eliminated the restriction on the phase number of a converter. In this scheme, the current flowing through the load can be equally divided in the respective phases and thereby achieving higher power ratings.

Inverters with the number of phases more than three are gradually coming into existence. Preferably, the five phase voltage source inverter (VSI) fed drives have many advantages over the three phase system. The increased number of phases directly results in an output voltage waveform with relatively less total harmonic distortion (THD). The five phase VSI fed induction motor has reduced amplitude of torque pulsations and increased frequency of torque pulsations compared to the three phase induction motor [1]. For the constant power output of the machine, the stator current per phase is also reduced and higher average torque per rms current can be achieved for the same size of an equivalent three phase machine. Thus, it leads to the quiet operation of the five phase machine and it is more fault tolerant. Even in the absence of one or more phases, the five phase motor effectively drives the load with minimum speed fluctuation.

Five phase inverter fed drives are highly suitable for standalone applications like electric hybrid vehicles, aerospace applications and ship propulsion that require high levels of reliability and efficiency. The third harmonic in a five phase system can be used to effectively reduce the torque pulsations in the steady state operation and the percentage of the third harmonic included along with the fundamental can be altered by the switching algorithm itself. In this paper, a novel and computationally efficient algorithm is worked out to independently control the fundamental and the third harmonic component of the voltage waveform in a five phase VSI.

## II. SVPWM GENERATION

The space vector pulse width modulation (SVPWM) is more preferable over the traditional sine pulse width modulation (SPWM) in a five phase VSI for the following reasons. There is increased utilization of the DC bus voltage in SVPWM as the zero vectors do not cancel each other out in SPWM. The main feature of a five phase VSI is the inclusion

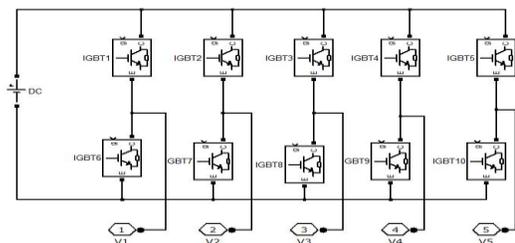


Fig. 1. Schematic of a five phase VSI

of the third harmonic component with the fundamental and this is tedious in SPWM.

The schematic of a five phase VSI is shown in Fig. 1. The voltages at the centre of the leg are expressed in terms of modulation signals  $g_i$ ,  $i=1,2..5$  where  $g_i$  is the modulation signal corresponding to the top device. It can be expressed as follows.

$$V_i = V_{dc} \left[ \frac{4}{5} g_i - \frac{1}{5} (\sum_{j=1, j \neq i}^5 g_j) \right] \quad (1)$$

#### A. Concept of a space vector

A space vector is a fictitious vector in space which uniquely determines a switching state of a power electronic device, in this case, an inverter. There are  $2^5=32(00000-11111)$  states in a five phase VSI out of which, 00000 and 11111 are termed as zero states. The remaining 30 states are termed as active states and they can be used to synthesize the output voltage wave. There are  $2*5=10$  sectors in a five phase VSI where each vector has eight states (2 zero states and 6 active states) and each active state is a part of two sectors. As the space vector is represented in a 2-D plane, the five phase voltages of the five phase VSI has to be transformed using the power variant transformation [2]. The transformation should be orthogonal [3] and hence the five quantities are transformed to five other quantities, two in the  $q1-d1$  stationary reference frame, two in the  $q3-d3$  stationary reference frame and one zero sequence component.

#### B. $q1d1q3d3o$ transformation

The space vector diagram is constructed by calculating the magnitudes of the space vectors using the following formulae and plotting it in a plane.

$$V_{d1q1} = \frac{2}{5} V_{dc} (V_a + V_b \ell^{j2\pi/5} + V_c \ell^{j4\pi/5} + V_d \ell^{-j4\pi/5} + V_e \ell^{-j2\pi/5}) \quad (2)$$

$$V_{d3q3} = \frac{2}{5} V_{dc} (V_a + V_b \ell^{-j4\pi/5} + V_c \ell^{j2\pi/5} + V_d \ell^{-j2\pi/5} + V_e \ell^{j4\pi/5}) \quad (3)$$

where  $V_a$ ,  $V_b$ ,  $V_c$ ,  $V_d$  and  $V_e$  are equal to  $V_i$ ,  $i=1,2,3,4,5$  respectively and are obtained by substituting each of the 32 states in (1). After substituting all the states in (1), the following space vector diagrams are drawn.

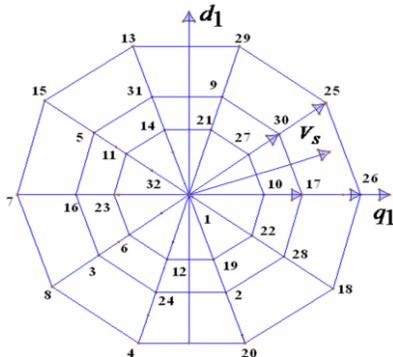


Fig. 2. Space Vector Diagram in the  $q1-d1$  stationary reference frame

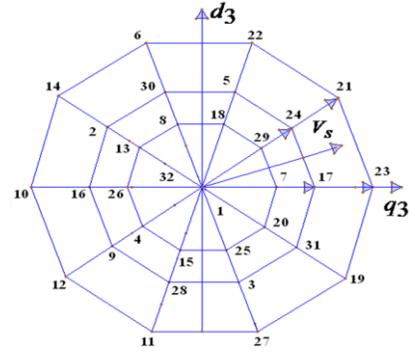


Fig. 3. Space Vector Diagram in the  $q3-d3$  stationary reference frame

The magnitudes of the vectors are given in Table 1. In Table 1,  $k = 0$  to 9 is the sector number with 0 starting from the positive x-axis.

TABLE I  
MAGNITUDES OF VECTORS IN THE SPACE VECTOR DIAGRAM

Vector	$q1-d1$ frame	$q3-d3$ frame
Large	$\frac{2}{5} V_{dc} 2 \cos(\frac{\pi}{5}) \ell^{j\frac{\pi}{5}k}$	$\frac{2}{5} V_{dc} 2 \cos(\frac{\pi}{5}) \ell^{j\frac{\pi}{5}k}$
Medium	$\frac{2}{5} V_{dc} \ell^{j\frac{\pi}{5}k}$	$\frac{2}{5} V_{dc} \ell^{j\frac{\pi}{5}k}$
Small	$\frac{2}{5} V_{dc} 2 \cos(\frac{2\pi}{5}) \ell^{j\frac{\pi}{5}k}$	$\frac{2}{5} V_{dc} 2 \cos(\frac{2\pi}{5}) \ell^{j\frac{\pi}{5}k}$
Zero	0	0

#### C. Modulation Strategy

In space vector PWM, the reference output voltage and frequency is first fixed. The reference wave is sampled at sampling frequency  $f_s$ . The inverter states, to be switched ON appropriately to construct the reference wave, are identified. This is done by first calculating the position of the reference wave in the space vector diagram and then finding the angle  $\alpha$  from the beginning of that sector. The duration of the two large vectors (outermost vectors) are then calculated by (4) and (5).

$$t_a = \frac{V_s t_s \sin(\frac{k\pi}{5} - \alpha)}{V_l \sin(\frac{\pi}{5})} \quad (4)$$

$$t_b = \frac{V_s t_s \sin(\alpha - \frac{(k-1)\pi}{5})}{V_l \sin(\frac{\pi}{5})} \quad (5)$$

where  $V_s$  is the reference output voltage,  $V_l$  is the magnitude of the large vector (obtained from Table I),  $t_s$  is the sampling period,  $\alpha$  is the angle between the reference wave and the beginning of the sector and  $k$  is the sector number.

The duration of the zero state  $t_0$  is found by subtracting (4) and (5) from  $t_s$  .(i.e.)

$$t_o = t_s - t_a - t_b \quad (6)$$

After  $t_a$ ,  $t_b$  and  $t_o$  are found out, their corresponding states are turned ON as per the timing diagram. The timing diagram is appropriately formed such that only one top switching device changes its state between states. The timing diagram for sector 1 is presented in Fig. 4.

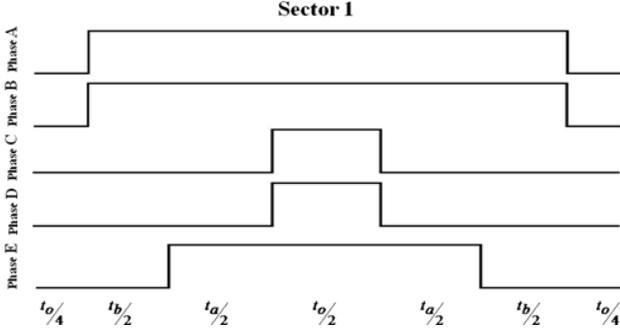


Fig. 4. Modulation signals for the top devices in a leg in sector 1

The same procedure is repeated for all the ten sectors using the outermost vectors. The maximum permissible reference voltage with large vectors alone  $V_{sl \max}$  is the radius of the largest circle that can be inscribed in the decagon.

$$V_{sl \max} = \frac{2}{5} V_{dc} 2 \cos\left(\frac{\pi}{5}\right) \cos \frac{\pi}{10} = 0.61554 V_{dc}$$

The above method has one major drawback, i.e. the output reference voltage which is synthesized has triplen harmonics. The occurrence of triplen harmonics is explained using Fig. 5. The states are numbered from 1 to 32, where 00000 and 11111 correspond to 1 and 32 respectively in Fig. 5.

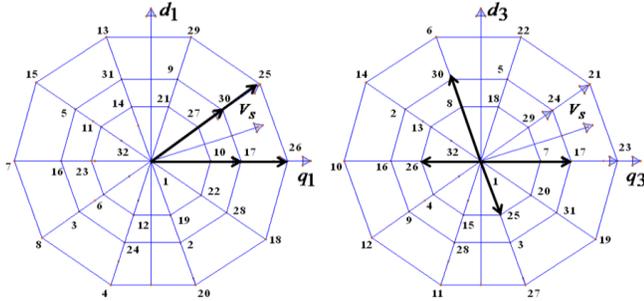


Fig. 5. Representation of the active states in sector 1 in the two  $q-d$  spaces

As it clear from Fig. 5, the active states (indicated in bold black) in the  $q1-d1$  space do not cancel each other out in the  $q3-d3$  space and hence triplen harmonics are present in the output. This problem can be overcome by using four vectors in a state instead of two and hence turning the medium vectors and the large vectors ON in such a way that the two vectors cancel out in the  $q3-d3$  space. This solution also stems from the fact that at least  $n-1$  vectors are required to construct a sinusoidal waveform for an  $n$ -phase inverter employing SVPWM [4]. The algorithm has been revised after the inclusion of medium along with the large vectors. Equations (4)-(6) are still used. The timings  $t_a$  and  $t_b$  are split into  $t_{al}$ ,  $t_{am}$  and  $t_{bl}$ ,  $t_{bm}$  respectively where  $t_{il}, i = a, b$  and

$t_{im}, i = a, b$  represents the ON time of the large vectors and medium vectors respectively. It can be expressed in (7) and (8).

$$t_{il} = p t_i, i = a, b \quad (7)$$

$$t_{im} = (1-p) t_i, i = a, b \quad (8)$$

For perfect sinusoidal output  $p$  should be equal to

$\frac{V_l}{V_l + V_m}$  such that the medium vector and large vector cancel out in the  $q3-d3$  space. When  $p=1$ , the large vectors alone are used. The timing diagram with the inclusion of medium vectors is presented in Fig. 6.

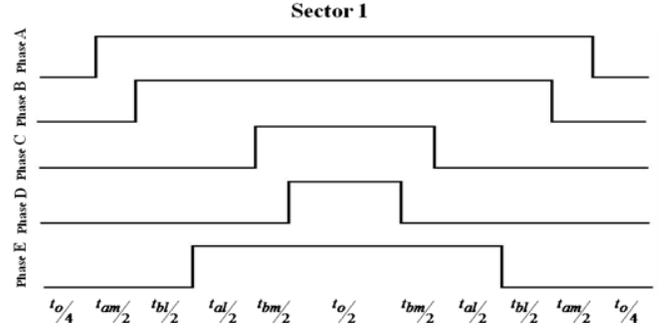


Fig. 6. Modulation signals for the top devices in a leg in sector 1

The maximum permissible reference output voltage decreases gradually as the shape becomes closer to a sine wave. It can be calculated as follows. The volt-second balance for the large vectors alone is compared with the volt-second balance with the inclusion of medium vectors.  $V_{sl}$  represents the reference voltage with large vectors alone and  $V_{slm}$  represents the reference voltage with medium and large vectors. This is expressed in (9) and (10).

$$V_{sl} t_s e^{j\alpha} = t_a V_{al} + t_b V_{bl} \quad (9)$$

$$V_{slm} t_s e^{j\alpha} = t_{am} V_{am} + t_{al} V_{al} + t_{bm} V_{bm} + t_{bl} V_{bl} \quad (10)$$

After the substitution of (4) to (8) in (9) and (10),  $V_{slm}$  is found to be,

$$V_{slm} = 0.8541 V_{sl}$$

It is found that the maximum permissible output voltage with large and medium vectors,  $V_{slm \max}$  has considerably decreased with the inclusion of the medium vectors.

$$V_{slm \max} = 0.5257 V_{dc}$$

### III. SIMULATION AND ANALYSIS USING MATLAB/SIMULINK

The SVPWM technique is implemented by using the instantaneous amplitudes of the reference phase voltages. In this method, five sinusoidal waves  $V_a$ ,  $V_b$ ,  $V_c$ ,  $V_d$  and  $V_e$  representing the output phase-neutral voltage is sampled dynamically at a sampling period  $t_s$ . The idea of this approach is to dynamically calculate the turn-on times of the top devices with respect to the sampled voltages. If the



TABLE II  
RELATIONSHIP BETWEEN  $m_r$  AND THE AMOUNT OF THIRD HARMONIC

S.No	$m_r$	Percentage of third harmonic(% of the fundamental)
1	0.00	00.09
2	0.25	06.52
3	0.50	12.54
4	0.75	18.31
5	1.00	23.52

The flowchart of the algorithm is shown below.

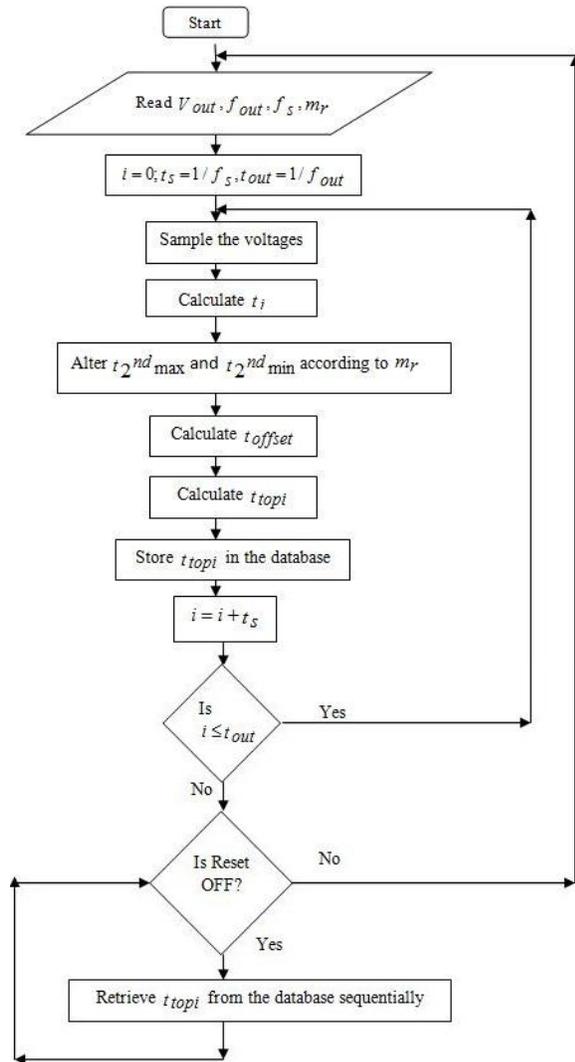


Fig. 10. Flowchart of the algorithm implemented

As shown in Fig. 10, the calculations are done for one period and the data is retrieved from the database periodically as long as the reset switch is OFF. Pressing the reset button breaks the infinite loop and takes the program to the first step and the entire process repeats.

### A. Power Supply Circuit

The power supply circuit of a five phase VSI contains ten 230/9 V, 500 mA step-down transformers, one 230/5 V, 750 mA step-down transformer and one 230/18 V, 1 A step-down transformer. The 230/9 V transformers provide the supply for the ten optocouplers. The 230/5 V transformer provides the supply for the PIC and the 230/18 V transformer provides the supply for the DC bus. An 18 V rectifying circuit with a C filter provides the 18 V DC bus voltage to the power circuit shown in Fig. 12.

### B. PIC and Isolator Circuit

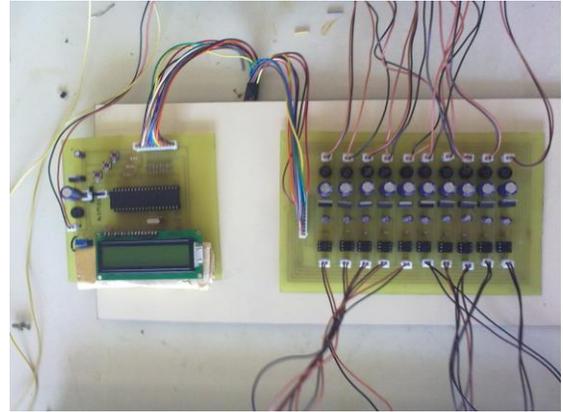


Fig. 11. PIC and isolator circuit of a five phase VSI.

The PIC circuit consists of PIC18f4550 microcontroller interfaced with a JHD162A LCD display and three push buttons for setting the input parameters. Output voltage, output frequency and sampling frequency can be set to a definite value using three push buttons. Based on these input parameters, PIC generates appropriate gating signals to the MOSFETS (IRF740) in the legs of the five phase VSI. As the PIC cannot drive the MOSFETS directly, isolator circuits are required. An optocoupler circuit acts as the isolator. It consists of ten gating signals that are generated by the PIC, each connected to an optocoupler biased by 12 V. The optocouplers conduct when the signal from the PIC goes high.

### C. Power Circuit

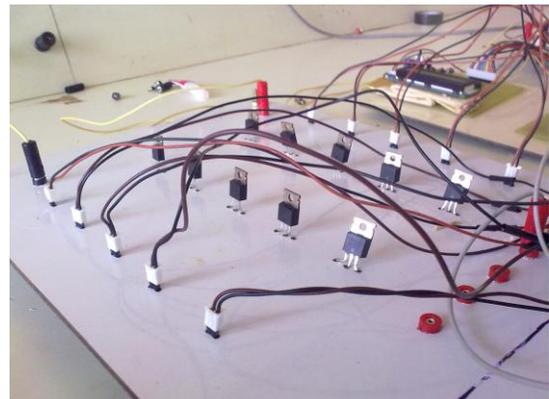


Fig. 12. Power circuit of a five phase VSI.

The power circuit of a five phase VSI has five arms with two MOSFETs in each arm. SVPWM based gating signals generated by PIC 18F4550 is given to gate of these devices through the optocoupler circuits. Necessary precautions are taken during the PCB fabrication and the connections of devices. The gating signals are obtained via 2-pin connectors as shown in Fig. 12. The appropriate connections are made such that the gating signal to a given MOSFET is the NOT of the other one in the same leg and the gating signals in the adjacent legs have a phase shift of  $\frac{2\pi}{5}$  radians corresponding to the required five phase output. Five phase output is taken at the centre of each leg shown in Fig. 12.

## VI. EXPERIMENTAL RESULTS

Using the three push buttons present on the hardware, a user interface is designed with the help of PIC microcontroller. The first button is used to increment any value displaying on the screen. The second button is used to decrement any value displaying on the screen. The third button allows the user to set the value and proceed to the next step. The final choice in data set while waiting for confirmation to proceed to the next step is shown in Fig. 13.



Fig. 13. LCD display showing all variables set by the user and asking for confirmation.

The output of the inverter is seen across a star connected resistance. The phase to neutral voltage across two resistances are taken and shown on a two channel DSO. This allows us to visualize the  $\frac{2\pi}{5}$  phase difference between adjacent phases. Fig. 14 shows output phase voltages,  $V_a$  and  $V_b$  employing the SVPWM technique at 50 Hz at a modulation index of 0.93. There is a phase difference of  $\frac{2\pi}{5}$  between the two waves.

## VII. CONCLUSION

The mathematical modeling of five phase SVPWM based VSI is worked out in this project. The VSI circuit based on SVPWM algorithm is simulated using MATLAB/SIMULINK and the results have been verified with [2]-[4] and found to be satisfactory. The same has been implemented using PIC 18F4550. The results obtained from the hardware are found to be satisfactory and almost matching with the simulation output waveform patterns.

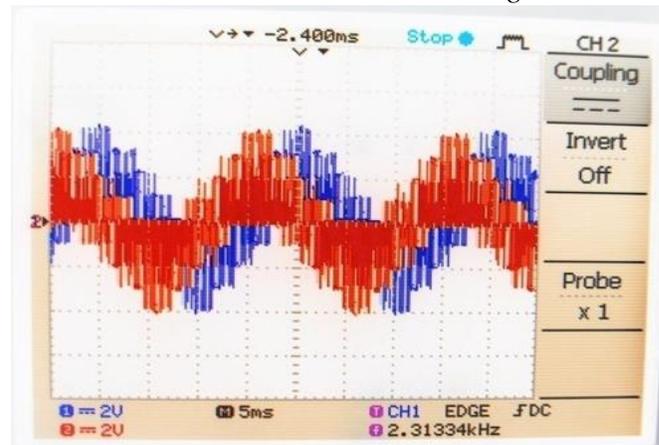


Fig. 14. Phase to neutral voltages of  $V_a$  and  $V_b$  employing SVPWM technique at 50 Hz and modulation index of 0.93.

The following conclusions are arrived with valid assumptions in the mathematical models; a) Inclusion of harmonics is possible to gain selected advantages, b) Utilization factor of the output waveform improves with the implementation of SVPWM based VSI, c) Switching losses are minimized as optimum switching is possible using space vector algorithm, and d) Very importantly, the total cost of the hardware is considerably minimized.

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